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For: METHOD AND SYSTEM OF CHARACTERIZING A DEVICE
UNDER TEST

1   1.   A method of characterizing a device under test, the method comprising:

2   injecting a signal into the device under test;

3   measuring the response to the injected signal to determine the impedance

4   of the device under test in the frequency domain;

5   converting the impedance of the device under test to a time domain; and

6   calculating the voltage noise of the device under test based on the

7   impedance in the time domain.

1   2.   The method of claim 1 in which the step of measuring the response

2   includes constructing an s-parameter matrix and calculating the real and imaginary

3   portions of the impedance of the device under test as a function of frequency based on the

4   s-parameter matrix.

1   3.   The method of claim 2 in which the step of construction the s-parameter

2   matrix includes establishing calibration data, generating an uncorrected s-parameter

3   matrix based on the measured impedance of the device under test, and applying the

4   calibration data to the uncorrected s-parameter matrix to produce a corrected s-parameter

5   matrix.

1   4.   The method of claim 1 in which converting includes performing an

2   inverse Fourier transform on the impedance in the frequency domain.

1   5.   The method of claim 1 in which calculating the voltage noise of the device

2   under test includes convolving the impedance in the time domain with a predetermined

3   current in the time domain.

1   6.   The method of claim 1 in which the impedance determined is self-

2   impedance.

1   7.   The method of claim 6 in which the step of determining the impedance of

2   the device under test includes measuring, at a terminal pair of the device under test using

3   one test port of an analyzer, the response to a signal input to the terminal pair from a

4   different test port of the analyzer.

1   8.   The method of claim 1 in which the impedance determined is the transfer

2   impedance.

1   9.   The method of claim 8 in which the step of determining the impedance of

2   the device under test includes measuring, at one terminal pair of the device under test

3   using one test port of an analyzer, the response to a signal input to a different terminal

4   pair of the device under test from a different test port of the analyzer.

1   10.   The method of claim 1 in which the voltage noise calculated is the

2 simultaneous switching noise.

1   11. The method of claim 10 in which the step of determining the impedance of

2 the device under test includes injecting an input signal to a plurality of terminal pairs of

3 the device under test.

1   12. The method of claim 11 in which the voltage noise at a particular terminal

2 pair of interest on the device under test is calculated and the simultaneous switching noise

3 is the sum of all voltage noise signals.

1   13. The method of claim 1 in which the device under test has multiple

2 terminal pairs and the timing of calculated voltage noise of each terminal pair is adjusted

3 until a maximum total voltage noise is achieved to determine a worst case scenario

4 concerning timing of the signal input to each terminal pair and the resulting total voltage

5 noise.

1   14. The method of claim 1 further including the step of determining the

2 spectral response of the device under test.

1   15. The method of claim 14 in which the step of determining the spectral

2 response of the device under test includes performing a Fourier transform on the

3 calculated voltage noise of the device under test.

1   16.   The method of claim 1 in which the device under test is a printed circuit

2   board.

1   17.   The method of claim 1 in which the device under test is an integrated

2   circuit package.

1   18.   The method of claim 1 in which the device under test is an interconnect

2   component.

1   19.   The method of claim 1 in which the device under test is a digital

2   representation of a physical device and the injected signal and measured response are

3   simulated.

1   20.   A method of characterizing a device under test, the method comprising:

2   determining the impedance of the device under test in the frequency

3   domain by constructing an s-parameter matrix and calculating the real and imaginary

4   portions of the impedance based on the s-parameter matrix;

5   converting the frequency domain impedance of the device under test to a

6   time domain by performing an inverse Fourier transform on the determined complex

7   impedance; and

8   calculating the voltage noise of the device under test by convolving the

9   time domain impedance with a predetermined current in the time domain.

1   21.   The method of claim 20 in which determining the impedance includes

2   injecting a signal into the device from one or more test ports of an analyzer and

3   measuring the response of the device.

1   22.   The method of claim 20 in which the predetermined current is a current

2   specified for the device under test.

1   23.   The method of claim 20 in which the step of constructing the s-parameter

2   matrix includes establishing calibration data, generating an uncorrected s-parameter

3   matrix based on the measured impedance of the device under test, and applying the

4   calibration data to the uncorrected s-parameter matrix to produce a corrected s-parameter

5   matrix.

1   24. The method of claim 20 in which the impedance determined is self-

2   impedance.

1   25. The method of claim 20 in which the step of determining the impedance of

2   the device under test includes measuring, at a terminal pair of the device under test using

3   one test port of an analyzer, the response to a signal input to the terminal pair from a

4   different test port of the analyzer.

1   26. The method of claim 20 in which the impedance determined is the transfer

2   impedance.

1   27. The method of claim 26 in which the step of determining the impedance of

2   the device under test includes measuring, at one terminal pair of the device under test

3   using one test port of an analyzer, the response to a signal input to a different terminal

4   pair of the device under test from a different test port of the analyzer.

1   28. The method of claim 20 in which the voltage noise calculated is the

2   simultaneous switching noise.

1   29. The method of claim 28 in which the step of determining the impedance of

2   the device under test includes measuring the response of a plurality of terminal pairs of

3   the device under test.

1   30.   The method of claim 29 in which the voltage noise of each terminal pair of

2   the device under test is calculated and the simultaneous switching noise is the sum of the

3   voltage noise of each terminal of the device under test.

1   31.   The method of claim 20 in which the device under test has multiple

2   terminal pairs, a signal is input to each terminal pair, and the calculated voltage noise of

3   each terminal pair is adjusted until a maximum total voltage noise is achieved to

4   determine a worst case scenario concerning timing of the signal input to each terminal

5   pair and a resulting total voltage noise.

1   32.   The method of claim 20 further including the step of determining the

2   spectral response of the device under test.

1   33.   The method of claim 32 in which the step of determining the spectral

2   response of the device under test includes performing a Fourier transform on the

3   calculated voltage noise of the device under test.

1   34.   The method of claim 20 in which the device under test is a printed circuit

2   board.

1   35.   The method of claim 20 in which the device under test is an integrated

2   circuit package.

1   36.   The method of claim 20 in which the device under test is an interconnect

2   component.

1   37.   The method of claim 20 in which the device under test is a digital

2   representation of a physical device.

1 38. A system for characterizing a device under test, the system comprising:

2   an input subsystem configured to inject a signal into the device under test

3 and measure the response of the device under test;

4   a routine responsive to the input subsystem for characterizing the

5 frequency domain impedance of the device under test;

6   a routine configured to convert the frequency domain impedance to a time

7 domain impedance; and

8   a routine configured to calculate the voltage noise of the device under test

9 based on the time domain impedance.

1 39. The system of claim 38 in which the input subsystem includes a network

2 analyzer.

1 40. The system of claim 39 in which the network analyzer includes a plurality

2 of test ports connectable to the device under test for injecting a signal into the device

3 under test and receiving a response from the device under test.

1 41. The system of claim 38 further including an output device for outputting

2 the calculated voltage noise of the device.

1 42. The system of claim 38 further including a user interface for inputting a

2 current specified for the device under test.

1   43.   The system of claim 38 in which the routine for characterizing the

2   frequency domain impedance is configured to construct an s-parameter matrix and to

3   calculate the real and imaginary portions of the impedance based on the s-parameter

4   matrix.

1   44.   The system of claim 43 further including a calibration routine for

2   establishing calibration data, an uncorrected s-parameter matrix is based on the measured

3   impedances of the device under test, and the calibration data is applied to the uncorrected

4   s-parameter matrix to produce a corrected s-parameter matrix.

1   45.   The system of claim 38 in which the routine configured to convert the

2   frequency domain impedance to a time domain impedance performs an inverse Fourier

3   transform on the frequency domain impedance.

1   46.   The system of claim 38 in which the routine for calculating the voltage

2   noise of the device under test convolves the time domain impedance with a

3   predetermined current.

1   47.   The system of claim 38 in which the impedance determined is self-

2   impedance.

1   48.   The system of claim 38 in which the input subsystem is configured to

2   measure, at a terminal pair of the device under test using one test port of the input

3   subsystem, the response to a signal input to the terminal pair from a different test port of

4   the input subsystem.

1   49.   The system of claim 38 in which the impedance determined is the transfer

2   impedance.

1   50.   The system of claim 49 in which the input subsystem is configured to

2   measure, at one terminal pair of the device under test using one test port of the input

3   subsystem, the response to a signal input to a different terminal pair of the device under

4   test from a different test port of the input subsystem.

1   51.   The system of claim 38 in which the voltage noise calculated is the

2   simultaneous switching noise.

1   52.   The system of claim 51 in which the input subsystem is configured to

2   input a signal to a plurality of terminal pairs of the device under test.

1   53.   The system of claim 52 in which the voltage noise at a particular terminal

2   pair of interest on the device under test is calculated and the simultaneous switching noise

3   is calculated as the sum of all voltage noise signals.

1   54.   The system of claim 38 in which the device under test has multiple

2   terminal pairs, a signal is input to each terminal pair by the input subsystem, and the

3   voltage noise at a particular terminal pair of interest is calculated and the timing of the

4   input signals is adjusted until a maximum total voltage noise is achieved to determine a

5   worst case scenario concerning timing of the signal inputs to each terminal pair and a

6   resulting total voltage noise.

1   55.   The system of claim 38 further including a routine for determining the

2   spectral response of the device under test.

1   56.   The system of claim 55 in which the routine for determining the spectral

2   response of the device under test performs a Fourier transform on the calculated voltage

3   noise of the device under test.

1   57.   The system of claim 38 in which the device under test is a printed circuit

2   board.

1   58.   The system of claim 38 in which the device under test is an integrated

2   circuit package.

1   59.   The system of claim 38 in which the device under test is an interconnect

2   component.

1   60.   The system of claim 38 in which the device under test is a digital

2   representation of a physical device and the input subsystem simulates an injected signal

3   and a response.

1   61.   A system for characterizing a device under test, the system comprising:

2   a routine for determining the frequency domain impedance of the device

3   under test by constructing an s-parameter matrix and calculating the real and imaginary

4   portions of the impedance based on the s-parameter matrix;

5   a routine for converting the frequency domain impedance to a time

6   domain impedance by performing an inverse Fourier transform on the complex

7   impedance; and

8   a routine for calculating the voltage noise of the device under test by

9   convolving the time domain impedance with a predetermined current.

1   62.   The system of claim 61 in which further including an analyzer configured

2   to inject a signal into the device from one or more test ports and to measure the response

3   of the device.

1   63.   The system of claim 61 in which the predetermined current is a current

2   specified for the device under test.

1   64. A system for characterizing a device under test, the system comprising:

2   an input subsystem configured to inject a signal into the device under test

3 and to measure the response of the device under test; and

4   a routine for automatically determining the frequency domain impedance

5 of the device under test by constructing an s-parameter matrix and calculating the real

6 and imaginary portions of the impedance based on the s-parameter matrix.

1   65. The system of claim 64 further including a routine for converting the

2 frequency domain impedance to a time domain impedance by performing an inverse

3 Fourier transform on the complex impedance.

1   66. The system of claim 65 further including a routine for calculating the

2 voltage noise of the device under test by convolving the time domain impedance with a

3 predetermined current.